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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/659,182 | 09/10/2003 | Dean D. Gans | MICS:0056-1/FLE 00-0301.0 | 7491 |

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| EXAMINER | |
|---|---|
| NGUYEN, VIET Q | |
| **ART UNIT** | **PAPER NUMBER** |
| 2818 | |

DATE MAILED: 12/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/659,182 | GANS ET AL. | |
| | Examiner | Art Unit | |
| | Viet Q Nguyen | 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *Pre-amendment filed on 9/10/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13 and 17-33* is/are pending in the application.

4a) Of the above claim(s) *14-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 17-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/10/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Applicant election of group claims **1-13 and 17-21** is acknowledged.

New claims 22-33 are added.

Claims **1-13, and 17-23** are now present for examination.

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **1-13, and 17-33** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakao (6,741,511) and.

Nakao (see Fig.2) clearly shows a memory system having a plurality of column memory blocks (CBK0 to CBKn) to store data, and a main column control circuit for simultaneously controlling such plurality of column/row, block access through corresponding local column control circuit (LCTL0 to LCTLn), and test mode signal (TMOD) for enabling the selection of said plurality column blocks through said corresponding local column control circuits. Fig.25 further shows another embodiment in which said test mode signal TMOD (shown as going into gate 110) is also used to activate a column block through a writing access with the use of write driver circuit (25). Fig. 21 then shows there are data lines (GIO) coupled between the write driver circuit (WRD) and the plural column blocks

(CBK0 to CBKn) such that data can be written to the memory blocks under control of the write driver output signals. Thus, it is obviously seen that this test mode signal also provides the write access to each of the block, and to generate the write enable signal (MWDE) for the selected particular block as desired. Furthermore, any test purpose can be carried out and including any burn-in test if desired.

It is further noted that Col. 27 (lines 5-10) mentions that "***it is possible... to select a plurality of row blocks simultaneously***, for connecting a plurality of local data line pairs one global data line pair", which also obviously suggest that a possible claimed configuration in which ***a global block select signal can select a plurality of memory blocks simultaneously*** so that said plural blocks may receive data from the write driver (25, Fig.25) at the same time, if any as similarly recited by the claims.

Fig. 10 shows at least one logical device (LCTL), in form of NAND gates (56) for receiving one or more internal column block (CBSFi) signals (from the input address signals (CAZ) signals from external source not shown), and for enabling the block signal (which also corresponds to a particular column block) to provide write access to the selected block as claimed based on said block signals. Note that such NAND gate (56) is configured to receive both an internal block select signal (CBSFi), for a selected particular block **"i"**, and a global test mode signal (TMOD) at the same time as claimed. When a plurality of block select signals (CBSFi) are generated for simultaneously select a plurality of column blocks, the

test mode signal TMOD will enable all the write drivers (see gate 55), corresponding to all selected blocks, and enable all the column block accesses (see gate 56) simultaneously as well during any burn-in write mode. Although "SRAM" is not mentioned in Nakao, such claimed features is considered as inherently because any memory device structure must use block decoding, access control, and write driver structure, and so Nakao has already shown a general decoding and write structure to be implemented in any type of memory design without undue experimentation or hardship on SRAM type. Also, the show circuits of Nakao also act as the means for performing the equivalent method steps of performance as recited in claims 14-21, respectively.

***Double Patenting***

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims **1, 2, 3, 5, 6, 7, 8, 9, 11, 12, 13** are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims **1, 2,**

**3, 1, 4, 5, 6, 7, 5, 8, and 9, respectively**, of U.S. Patent No. Gans et al (6,621,755). Although the conflicting claims are not identical, they are not patentably distinct from each other because both set of claims contain similar claim language as also drawn toward a same invention.

5. The cited references are considered pertinent to present application. Kuroki et al (6,751,128) and Ohbayashi et al (6,741,510) all shows the use of global block select signal to enable a plurality of memory blocks concurrently for simultaneously accesses.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

V. Nguyen
11/30/2004

Viet Q Nguyen
Primary Examiner
Art Unit 2818